Master's Thesis

12−14.5 GHZ DIGITALLY CONTROLLED OSCILLATOR USING A HIGH-RESOLUTION DELTA-SIGMA DIGITAL-TO-ANALOG CONVERTER

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Yong-Woo Jo

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Approved by

Advisor
Kyuho Lee

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ABSTRACT

This thesis focuses on the design of digitally-controlled oscillators (DCO) for ultra-low-jitter digital phase-locked-loops (PLL), which requires very fine frequency resolution and low phase noise performance. Before going details of the design, fundamentals of the digital-to-analog converter (DAC), delta-sigma modulator (DSM), *LC* voltage-controlled oscillator (VCO) are discussed in Chapters 2, 3, and 4 respectively. Detailly, Chapter 2 begins with the basic operations of the digital-to-analog converters. Plus, several types of DACs and their properties are discussed. For instance, resistor-based DAC or current source-based DAC. In Chapter 3, the backgrounds of DSMs are presented. The reason why DSMs are indispensable components in fractional number generation is presented. The meaning of the randomization and noise shaping in DSMs is discussed then high-order noise shaping DSMs are explained as well. Chapter 4, starts with the *LC* tanks. Integrated passive components are introduced such as spiral inductors, metal-insulator-metal (MIM) capacitors, and metal-oxide-metal (MOM) capacitors. The start-up of the oscillators also explained by using two approaches, the Barkhausen criterion and the negative resistance theory. Then the pros and cons of the CMOS and NMOS type topologies are stated. Finally, the phase noise in oscillators is analyzed by using the Leeson's equation and the impulse-sensitivity function theory. In chapter 5, the detailed designs of the prototype DCO are presented. The designed DCO consists of 2^{nd} order DSM, string resistor-based DAC, and CMOS-type *LC* VCO. The frequency resolutions of the proportional and integral path are different but the structures are identical. For the high-performance oscillator, iterative design is required. In the measurements, the designed DCO achieved 17 and 18 bit of frequency resolution in the proportional and integral path respectively, 12-14.5GHz of the frequency tuning range, 50 and 500MHz/V of KVCO for the main and auxiliary loop respectively, and -184.5 dB of figure of merit (FOM). The power consumption is 5.5mW and the prototype was fabricated in TSMC 65nm CMOS process.

CONTENTS

LIST OF FIGURES

1. INTRODUCTION

1.1. MOTIVATION AND RESEARCH OBJECTIVES

As the communication industry has developed rapidly over the last few decades, the research of related communication circuits has also received a lot of attention. From the aspects of commercialization, the most critical issues to be considered are small-area, and low-power designs while attaining required performance. With the recent trend that the fabrication process to be more suitable for digital designs, digital designs with small-area, low-power design to meet market requirements are attracted. Digital-based designs also have the advantage of its reconfigurability and easiness of redesign as process scales.

All-Digital Phase-Locked-Loops (ADPLL) have been intensively explored due to the above features. However, the quantization noise due to the limited frequency resolution of frequency discretization in digitally-controlled oscillators (DCO) can limit the performance of ADPLL in terms of out-band phase noise [1]. In order to achieve a very fine frequency resolution, such that the quantization noise is lower than the phase noise of oscillator, the size of the minimum adjustable switched capacitor must be smaller than several atto-Farads, which is limited by the process technology [1]. Recently, some research attempts to minimize the effective adjustable switched capacitor such as capacitive divider networks [2] or C-2C switched-capacitor ladder [3]. However, both solutions are not robust in process variation because of their mismatches and parasitics. Another possible solution is exploiting the characteristics of the delta-sigma modulators (DSM), which is relatively insensitive to process variation.

Digitally-controlled oscillators (DCO) or Voltage-controlled oscillators (VCO) are the most important components in PLLs that determine the overall performance of the PLL. Therefore, it is very important to design an appropriate oscillator for design purpose. *LC* Oscillators usually occupy huge silicon area, however, because of its superior Figure-of-merit (FOM) due to its intrinsic frequency selectivity, it is widely adopted in high-performance RF applications. *LC* oscillators can be classified into Class-B, C, D, F, etc. by the conduction angle or harmonic characteristics. Among them, Class-B architecture is the most popular because of its design simplicity and reliability.

This thesis is oriented to analyze the DCOs and *LC* oscillators themselves. A prototype is fabricated to demonstrate our analysis and feasibility of DSM based high-resolution DCO.

1.2. THESIS ORGANIZATION

This thesis mostly focuses on DCOs that has high-frequency resolution while providing low phase noise and its components, i.e., DSM DAC and *LC* VCO. The organization of this thesis is as follows. Chapters 2 to 4 focuses on providing fundamentals.

In chapter 2, DAC fundamentals are introduced. Basic operation and various topologies such as resistor DACs and current-steering DACs are discussed.

Chapter 3, the basics of DSMs will be discussed including randomization and noise shaping characteristics.

Chapter 4, the basics of *LC* VCOs will be discussed. *LC* resonators, start-up, a variety of topologies and noise performance will be considered.

Chapter 5, explores the analysis and design of DCOs and describes an implementation of DCOs along with experimental results and design considerations.

Finally, chapter 6 summarizes all the materials that we discussed and proposes future research directions.

2. DIGITAL-TO-ANALOG CONVERTER (DAC) FUNDAMENTALS

2.1. BASIC OPERATING CHARACTERISTICS

Necessity of data converter circuits cannot be emphasized enough in analog-digital interface. There are two types of data converters, analog-to-digital converters (ADCs) and digital-to-analog converters (DACs). This thesis only focuses on DACs as a part of DCOs. To assess the performance of DACs, several characteristics are existing.

Resolution

Possible number of output levels, usually expressed in bits. N-bits DAC is capable of reproduce 2^N levels of output. Another expression of resolution is effective number of bits (ENOB). Ideally, N-bits DAC will capable of reproduce 2^N of output levels. However, real circuits and signals have additional distortion or noise. Because of the non-ideality, such as noise, effective resolution of N-bits DAC can be less than N-bits. So that N-bits DAC will not capable of reproduce 2^N of output levels anymore.

Monotonicity

The analog output always follows the sign of the digital input changes, a DAC is said to be monotonic. Monotonicity is a significant characteristic in communication applications. Some nonlinearity is acceptable, but with nonmonotonicity, such applications probably not working at all.

Linearity

There are two measures of linearity, differential nonlinearity (DNL) and integral nonlinearity (INL).

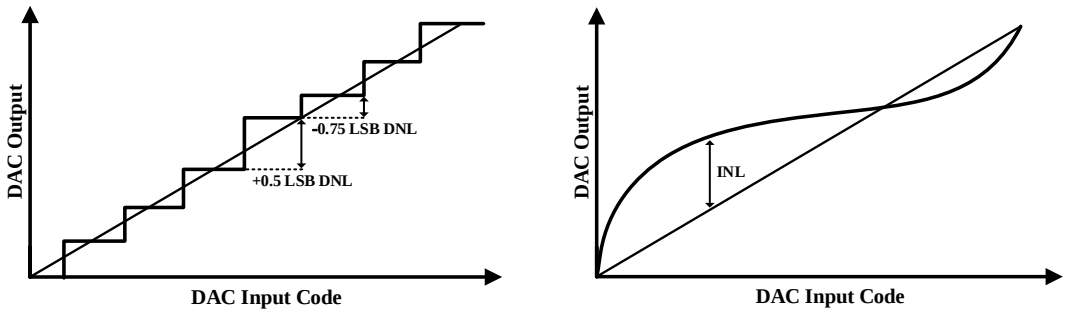

Figure 1. DNL and INL depiction.

In ideal DAC, any two sequential DAC codes is 1 LSB apart. DNL measures the worst-case deviation of any two sequential codes. By using DNL, monotonicity and missing code can be detected.

If DNL is less than or equal to −1, the DAC is considered as nonmonotonic. If DNL is greater than or equal to +1, the DAC has missing codes. INL, measures how the transfer function differ from ideal transfer function. INL is sometimes referred to as relative accuracy. INL only defines the DAC linearity and is typically used more often than DNL.

Maximum sampling frequency

The maximum frequency that the DACs can still operate and generate correct output.

2.2. RESISTOR DACS

Resistor DACs are one of the simplest form of DACs. This thesis only considers two configurations, string resistor ladders and R-2R resistor ladders.

2.2.1. STRING RESISTOR LADDERS

String resistor ladders, also known as Kelvin divider, consists of 2^n equal series resistors and 2^n switches between each node for n-bit DAC.

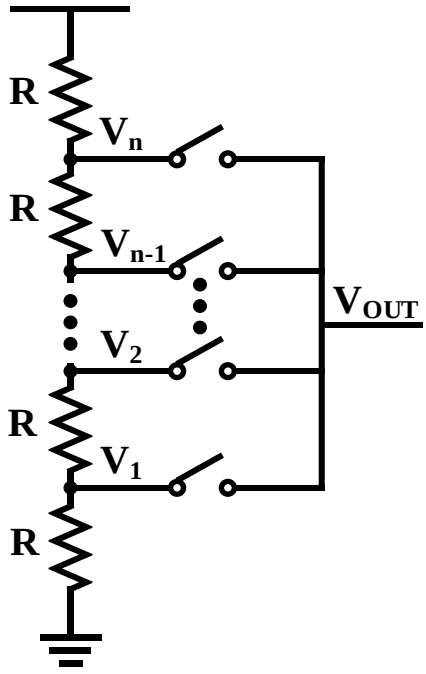

Figure 2. Topology of String resistor ladder.

Figure 2. shows simple topology of string resistor ladder. The output is taken from certain tap by closing one of the switches. This topology is simple and output voltage is inherently monotonic. The output impedance is code dependent so string resistor ladders suffer from nonlinear characteristic. Therefore, inserting OP-AMP to the output of the DAC is recommended to buffer output impedance so as provide a low impedance to the following block. The main drawback of string resistor ladders is, for the fine resolution, a huge number of resistor and switches is required. Suppose resolution is 12-bit, total 4086 resistors and switches would require. So, it is not favorable in high resolution applications.

2.2.2. R-2R RESISTOR LADDERS

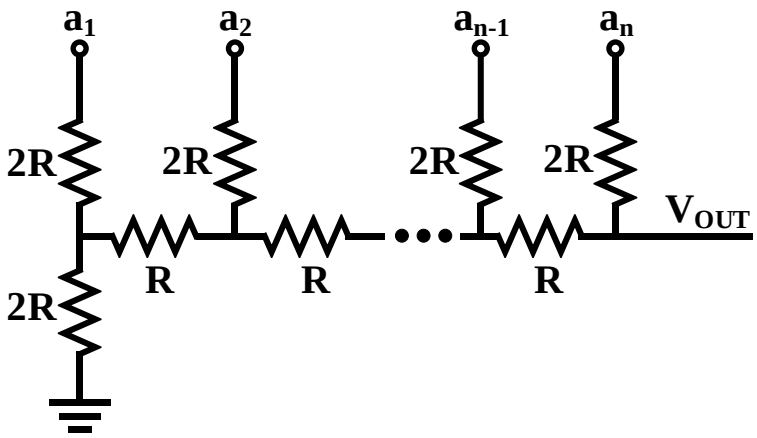

Figure 3. Topology of R-2R resistor ladder.

Figure 3. shows topology of R-2R resistor ladder. Bit a_1 is least significant bit, LSB and a_n is most significant bit, MSB. The bit inputs are switched between V_{LOW} (Logic 0) and V_{HIGH} (Logic 1). This R-2R, digital bits are weighted in their contribution to the output voltage. As the bits are set to 0 or 1, the output voltage will get a corresponding value between V_{LOW} and V_{HIGH} – minimal step. For the input digital code D_IN, with n-bits DAC, the output voltage V_{OUT} is:

$$V_{OUT} = V_{HIGH} \times \frac{D\_IN}{2^n} \tag{1}$$

Suppose, n = 8 and VHIGH is 1.2 V (nominal voltage for 65nm CMOS), maximum value of output voltage is 0.996 and minimum step is 0.004 V.

Unlike string topology, R-2R topology has advantage refer to costs when consider a high-resolution design. To increase the number of bits of DACs, string topology exponentially increases the number of resistors and switches, while the R-2R topology increases resistors and switches linearly. Therefore R-2R ladder occupy relatively small-area. However, R-2R topology has a critical point. R-2R ladder operates just like current dividers, and DAC output accuracy is dependent on the matching of resistors. Small deviation in the value of MSB resistors can entirely affects to the contribution of LSB resistors. This possibly results in nonmonotonicity at the point that MSB transitions. Consequently, R-2R type DAC also has a restriction in the resolution although the applications require the number of bits to more than 10 bits, typically limited to 8-bits.

2.3. CURRENT-STEERING DACS

Among the variety of DACs, the current-steering topology have the highest operating frequency then becomes a reliable solution for GHz applications[4].

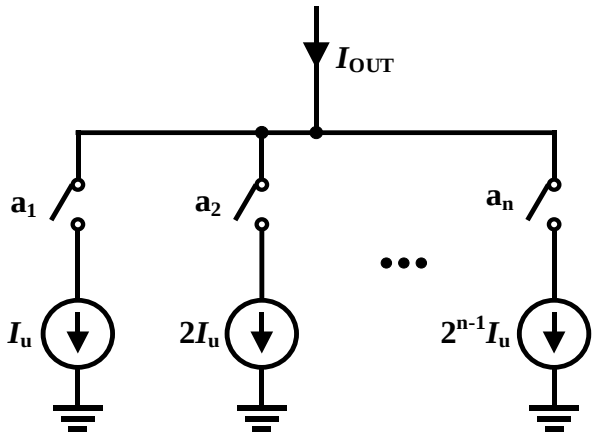

Figure 4. A simple binary-weighted current-switching DAC

Suppose we are going to convert n-bit digital code to an analog output, I_{OUT} as figure 4 shows. Each input bit controls a binary weighted current where the unit value is I_u. In here, a_1 denotes LSB and a_n denotes MSB. The output current becomes:

$$I_{OUT}=a_n(2^{n-1}I_u)+\cdots+a_2(2I_u)+a_1I_u \quad (2)$$

This circuit is current-switching DAC but not a current-steering DAC. This DAC has an important advantage over other types of DAC. It can drive resistive loads without a buffer, which is crucial when drives a transmission line or load has resistive components. However, the current-switching topology

suffers from dynamic error. When a switch turns off, the upper node of its corresponding current source discharges to zero. Then, next time, when this switch is enabled, the nonlinear parasitic capacitance at this node have to charge up. This draws a tremendous current from the output node. Even more, the ground voltage fluctuates a lot because the switching actions change the total current dynamically. To solve these defects of current-switching topology, current-steering topology is introduced.

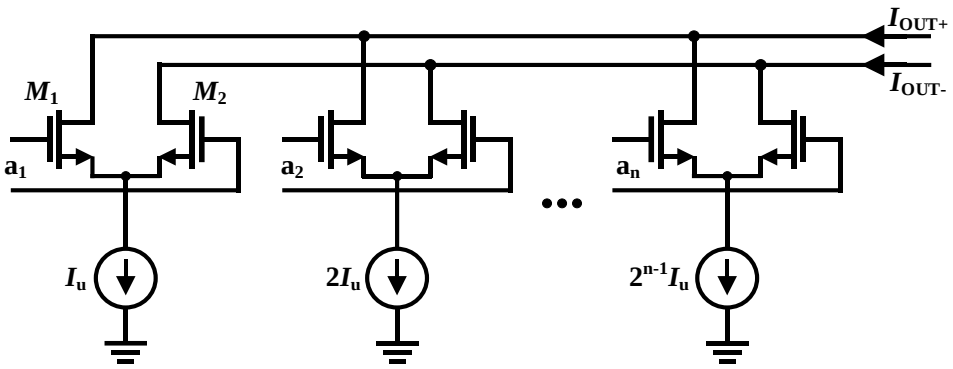

Figure 5. A simple binary-weighted current-steering DAC

The problems of current-switching topology can be successfully suppressed by use of current-steering topology (Figure 5). Thanks to the differential pair, the tail current is steered to the left or right, so that causes tiny voltage fluctuations at the upper node of current source. Moreover, since the current of DAC stays constantly, ground voltage does not fluctuate. One defect of current-steering DACs is the limited range of output voltage. Because the differential pair must operate at the saturation region. Another defect is that the input digital signal is not rail-to-rail regime to ensure that all the differential pair operates at the saturation reason as well which requires additional pulse generator.

3. DELTA-SIGMA MODULATOR (DSM) FUNDAMENTALS

3.1. BASIC OPERATING CHARACTERISTICS

Let us assume we have dual modulus frequency divider whose modulus is N and N+1. Then what if the modulus number is not constant and changes over time? For example, if N and N+1 appear same amount of time, effective modulus number is N+0.5. By changing the ratio of time, making any of fractional number is possible. However, the problem is pattern of changing order. As an instance, consider a dual modulus divider circuit where input frequency is 10 MHz and N is equals to 10. Let us say the divider divides by 10 for 9 reference term and by 11 for 1 reference term. The average output frequency is 1.1 MHz but shows a sort of pattern (periodicity) every 10 reference term and it becomes "fractional spurs" in frequency domain. This chapter, to compensate fractional spurs, delta-sigma modulator and its randomization and noise shaping characteristics will be discussed.

3.2. RANDOMIZATION

In the previous section, we have seen a periodicity and formation of fractional spurs. What if the modulus changes randomly while maintaining the average value to 10.1? Then the periodicity is broken and the fractional spurs is converted to noise. Next step is computing the noise. Assuming the divider has two modulus, N and N+1 and have an average modulus of N+α. Instantaneous modulus is denoted as N+b(t), b(t) is random variable a value of 0 or 1 randomly changes and its average value is α. The instantaneous divider out frequency is expressed as:

$$f_{\mathrm{DIV}}(t) = \frac{f_{\mathrm{VCO}}}{N+b(t)} \tag{3}$$

Ideally, $b(t)$ is equals to α and does not change. However, in real implementation, we approximate α by dithering 0 and 1, so that noise occurs. b(t) can be also express as followings:

$$b(t) = \alpha + q(t) \tag{4}$$

$q(t)$ is said the quantization noise and it shows the error occurred by $b(t)$ in approximating a fractional number.

3.3. NOISE SHAPING

3.3.1. BASIC NOISE SHAPING

To the expense of canceling the fractional spurs with modulus randomization, high phase noise has been increased. Such a high-level quantization noise originated from approximating a fractional value by using only two coarse values, 0 and 1 that the resolution is limited to 1. These days, modern applications solve this issue by shaping the phase noise to the high pass form.

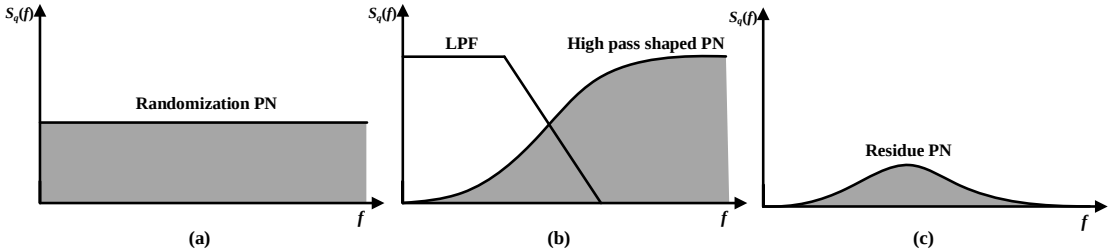

Figure 6. (a) Phase noise for fully randomized PN and (b) High pass shaped PN and LPF and (c) Residue PN

By using high pass shaping technique, quantization noise can be remarkably reduced as far as additional low pass filter is applied. Figure 6. shows noise transfer functions. By modulus randomization, fractional spurs are suppressed but phase noise aroused (a). High pass shaped phase noise and low pass filter transfer function to be convoluted (b) and the left-over phase noise (c) after applying low pass filter to the high pass shaped phase noise. Generating sequence $b(t)$ to make a high pass shaped noise is so called "noise shaping." We now consider noise shaping in z-domain with negative feedback system shown below in Figure 7.

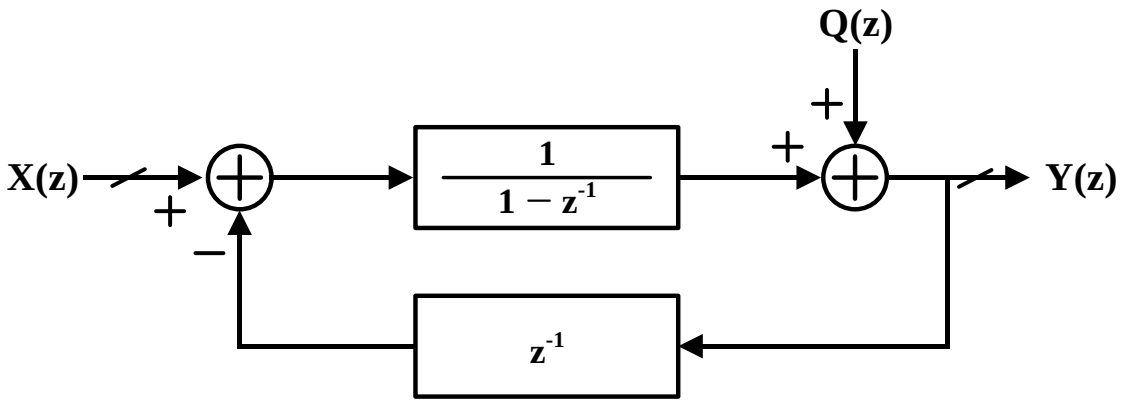

Figure 7. z-domain model of delta-sigma modulator (DSM)

X(z) represents input and Y(z) represents output of DSM. The number of bits of X(z) determines the resolution of DSM. The number of output bits determines the order of DSM. 1st order DSM has 1-bit output. The transfer function of 1st order DSM can be expressed as [5]:

$$Y(z) = X(z) + Q(z) \cdot (1 - z^{-1}) \tag{5}$$

Then by applying inverse z-transform, we can rewrite as when zero input:

$$\begin{aligned} \frac{Y(z)}{Q(z)} &= 1 - z^{-1} \\ &= e^{-j\pi ft} \left(e^{+j\pi ft} - e^{-j\pi ft}\right) \\ &= 2je^{-j\pi ft} \sin(\pi ft) \end{aligned} \tag{6}$$

Taking square both sides and noise transfer function (NTF) is earned as follows [RF]:

$$NTF(f) = |2 \sin(\pi ft)|^2 \tag{7}$$

This equation shows the high pass noise shaping characteristic.

3.3.2. HIGH-ORDER NOISE SHAPING

So far, we have explored basic noise shaping operation of 1st order DSM. The 1st order DSM sometimes is not sufficient to suppress the quantization noise. For the sufficient suppression, high order DSMs are needed. For the nth order DSMs, noise transfer function is:

$$\mathrm{NTF}(f) = |2\sin(\pi f t)|^{2n} \tag{8}$$

This equation implies that high order DSM shaping noise sharper compared to 1st order DSM.

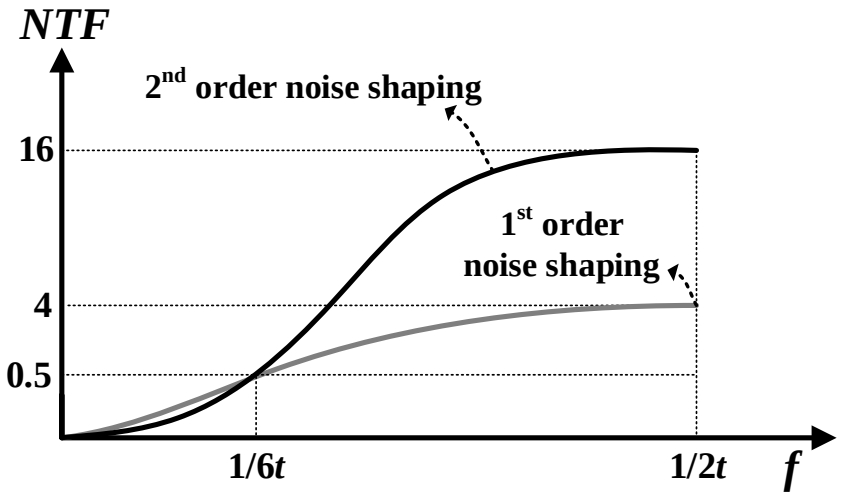

Figure 8. Noise shaping of 1st and 2nd order DSM

Figure 8. compares 1st order and 2nd order DSM. It is clear that 2nd order DSM has much more energy in higher frequency. Regardless of order of DSMs, they have common cross point, when frequency is 1/6t. To filtering out the higher order DSM, higher order low pass filter is necessary. Now, the output signal of 2nd order DSM toggles between -2, -1, 0, 1 unlike 1st order DSM.

4. *LC* VOLTAGE-CONTROLLED OSCILLATOR (VCO) FUNDAMENTALS

4.1. BASIC OSCILLATOR CHARACTERISTICS

These days, many communication applications prefer using *LC* VCOs for their low-power, low-jitter, wide-band performance. To asses the performance of VCOs, one integrated index in needed. Here, we have figure of merit (FoM) to compare the performance of VCOs and it is expressed as follows:

$$\mathrm{FOM} = \mathcal{L}(\Delta f) + 10\log\left(\frac{P}{1\mathrm{mW}}\right) - 20\log\left(\frac{f_c}{\Delta f}\right) \tag{9}$$

Where f_c, Δf, and P denotes center frequency, offset frequency and power dissipation of the VCOs. Base on this equation, various applications are possible. For example, when we consider frequency range (FTR) of the VCOs as well, FOMT is defined as below.

$$\mathrm{FOMT} = \mathcal{L}(\Delta f) + 10\log\left(\frac{P}{1\mathrm{mW}}\right) - 20\log\left(\frac{f_c}{\Delta f}\right) - 20\log\left(\frac{\mathrm{FTR}}{10}\right) \tag{10}$$

To maximize the FOM is quite tricky job since all the parameters are trade-off each other. Therefore, understanding the basic mechanism of *LC* VCOs is important. In this chapter, the very basics of the *LC* VCOs will be explained.

4.2. *LC* RESONATORS

Designing a *LC* tank is a milestone of *LC* VCOs design. Through the tank design, the oscillation frequency and phase noise level can be fixed. As shown in figure 9, the tank consists of an inductor, *L* and a capacitor, *C*. In the ideal tank (a) there is no lossy components however in practical design, we have to consider the tank as lossy tank (b).

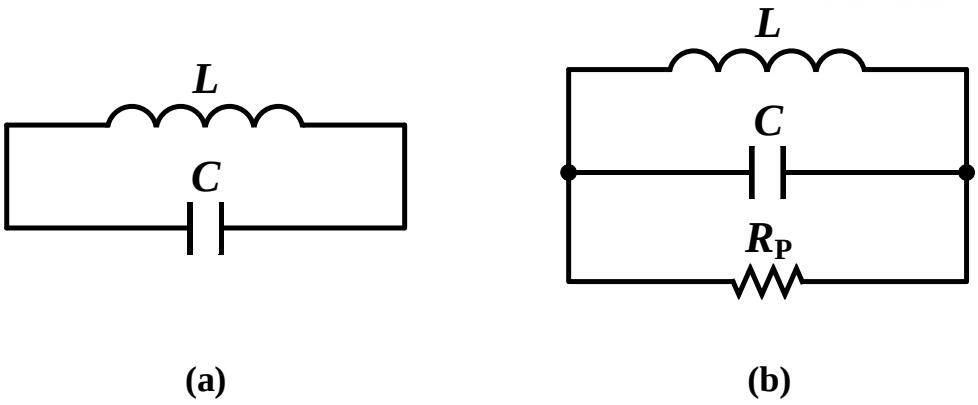

Figure 9. Ideal lossless *LC* tank (a) and practical lossy *LC* tank (b)

In practical tank, the lossy component is come from the parasitic resistance. Both cases have same resonance frequency where the tank impedance is maximized.

$$f_c = \frac{1}{2\pi\sqrt{LC}} \tag{11}$$

In the ideal case, at the resonance frequency, tank impedance goes to infinity but in ideal case, only R_p remains.

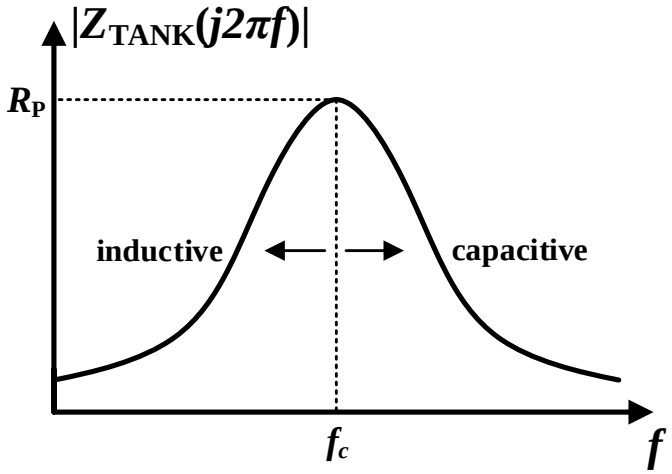

Figure 10. Magnitude response of tank impedance, $Z_{TANK}(j2\pi f)$

As shown in figure 10, tank impedance is maximized at the resonance frequency and its peak value is R_P. Below the resonance frequency, the inductor dominates the overall impedance and above the resonance frequency, capacitor dominates the overall impedance.

Quality factor (Q-factor) is one of the important parameters in *LC* VCOs. Q-factor indicates how much energy is stored in the tank and dissipated energy in the tank. If Q-factor of the tank is high, the tank has sharper magnitude response. Since the *LC* tank is a innated band pass filter, sharper response means filtering ability is enhanced. Therefore, a high Q-factor *LC* VCO has better phase noise performance since noises apart from the resonance frequency are more filtered out. The Q-factor of the passive components in the tank can be expressed as:

$$Q_{\mathrm{IND}} = \frac{R_{\mathrm{P}}}{j2\pi fL} = \frac{j2\pi fL}{R_{\mathrm{S}}} \tag{12}$$

$$Q_{\mathrm{CAP}} = R_P(j2\pi fC) = \frac{1}{R_{\mathrm{S}}(j2\pi fC)} \tag{13}$$

R_P is parallel resistance in parallel network, R_S is series resistance when we transform the tank to series network. Depending on the frequency bands, Q-factor dominator is different. In GHz band, inductor is dominating factor whereas in mmW band, capacitor is dominating factor. Therefore, design approach should be differentiated with frequency bands.

4.2.1. INTERGRATED INDUCTORS

In the designing of GHz *LC* VCOs, understanding characteristics of inductor is very critical since tank Q-factor is dominated by the inductor. Passive inductor seems to have constant value, however, in reality, inductance and Q-factor vary as operating frequency changes. At lower frequency, the series resistance of the inductor is constant. So, Q-factor follows the theoretical equation. And inductance is constant. At higher frequency, series resistance significantly increase as frequency goes up. The main cause of this phenomenon is skin effect. The skin depth of a good conductor is defined as:

$$\delta = \frac{1}{\sqrt{\pi f \mu \sigma}} \tag{14}$$

where the f, μ, and σ represent frequency of current, permeability, and conductivity of metal each. The skin depth and frequency has inverse proportional relationship. As the frequency increases, the skin depth decreases. Therefore, the effective series resistance increases since it has a same effect as effective cross section area of inductor metal decreasing. Moreover, the proximity effect has a similar effect. Therefore, at higher frequency, Q-factor steeply decreases. What about inductance? Inductance decreases as well since the parasitic capacitance of inductor resonates with inductance. That is, above

self-resonance frequency of inductor, inductor shows capacitive regime. So that, when considering ultra-high frequency *LC* VCOs such as mmW band, evading such phenomena is crucial. To push the self-resonance frequency away, multi metal stacking, fewer turns or wide width inductor can be considered.

4.2.2. INTEGRATED CAPACITORS

In the recent integrated circuits design, usually there are 3 kinds of capacitors generally used; metal-oxide-metal (MOM) capacitor, metal-insulator-metal (MIM) capacitor, and metal-oxide-semiconductor (MOS) capacitor. MOM and MIM capacitors are passive components and MOS capacitor is active component. Each capacitor has different characteristics therefore, it should be used on appropriate purpose.

Metal-oxide-metal (MOM) capacitors

The structure of MOM capacitors, also known as metal finger capacitors are shown in figure 11. MOM capacitors exploit the parasitic capacitance between metal plates and additional masks are not needed. MOM capacitors are wide used in advanced CMOS process since their higher capacitance density and lower cost compared to the other capacitors [6]. To further increase the capacitance density, multiple layers can be stacked then Q-factor increases as well as series resistance decreases. In addition, there are several variations of MOM capacitors [7]. When we place metal finger alternatively, capacitance density significantly increases and we call it alternate-polarity (AP) MOM capacitors. It is possible to insert vias between metal plates. This form is called vertical natural capacitors (VNCAP). Also, by rotating, fracture, etc. various geometry can be used.

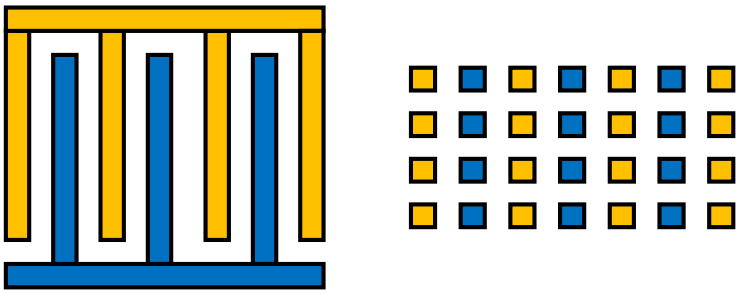

Figure 11. Top and cross section views of MOM capacitors

Metal-insulator-metal (MIM) capacitors

The MIM capacitors consists of two metal plates and insulator (dielectric material) between the plates. The upper metal plate is called capacitance top metal (CTM) and the bottom metal plate is called capacitance bottom metal (CBM). For higher capacitance density, the insulator is usually made by high-

k dielectric material. Because of this dielectric material, to implement MIM capacitors, additional fabrication masks are required that causes fabrication cost increasing. Despite its high manufacturing cost, it is widely chosen for its high linearity, robustness, and capacitance density.

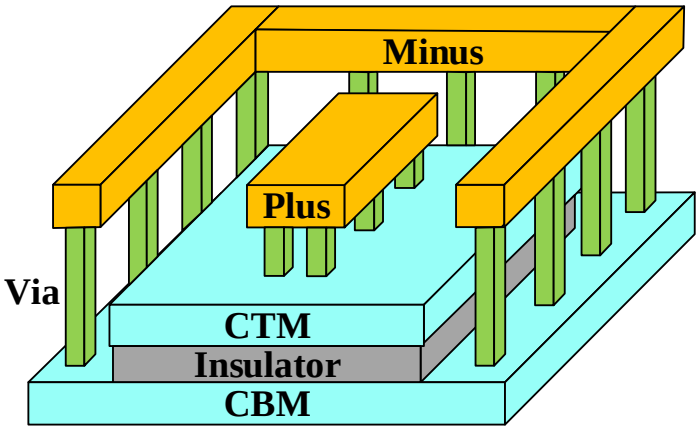

Figure 12. MIM capacitors schematics

Figure 12. show the schematics of MIM capacitors. Typically, thick metals are used in plus and minus terminals. Compared to MOM capacitors, as the distance between bottom plate and substrate is longer, the parasitic capacitance is smaller than that of MOM capacitors.

Metal-oxide-semiconductor (MOS) capacitors

MOS capacitors, usually called varactors, are the only active capacitors exploit the mechanism of field effect. The gate oxide is used as insulator and recent advanced CMOS process adopt high-k dielectric. Figure 13. shows accumulation mode NMOS based MOS capacitors which is most commonly used for its monotonicity. The reason why it is called accumulation mode capacitors is electrons always accumulates in the channel regardless of gate-source voltage since electron is majority carrier in n-well. Without n-well, NMOS based MOS capacitors suffer from nonmonotonicity. Because, when V_{GS} is negative value, hole accumulates in the channel and when V_{GS} is positive over the threshold voltage, electron inversion layer is formed in the channel. In both cases, capacitance increases, therefore, monotonicity vanishes. In PMOS based MOS capacitors, these mechanisms are similar but vice versa. MOS capacitors are as shown in figure 13, sensitive to the bias voltage and its C-V curve is nonlinear. In addition, thin oxide device suffers from moderate leakage current so that bias voltage changes in spite of its high capacitance density. Eventually, MOS capacitors are not chosen for the critical applications such as bypass capacitors.

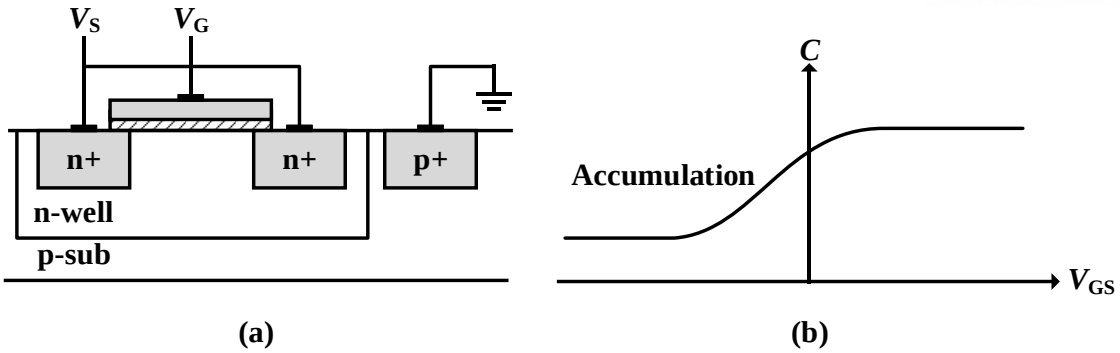

Figure 13. (a) Structure of accumulation mode MOS capacitors (b) C-V characteristics

4.3. START-UP OF *LC* VCOS

There are two approaches to understanding the start-up of *LC* VCOs. One is "Barkhausen criterion" and, the other is negative resistance.

Barkhausen criterion consider the oscillators as feedback system. Figure 14. shows the linear feedback model with a feedforward gain of $H(s)$. Using this model, Barkhausen criterion can be expressed as:

$$|H(s)| = 1$$
$$\angle\left(H(s)\right) = 2\pi n \qquad (15)$$

Where n is an integer value (1,2,3…). This implies that it the loop gain is unity and phase shift is integer multiplies of 2π, the feedback system can oscillate. Keep in mind that this criterion are not a sufficient condition but a necessary condition.

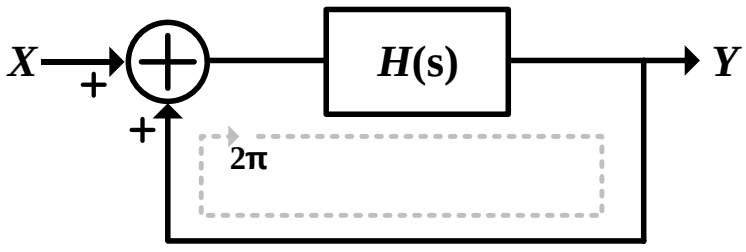

Figure 14. Feedback system with forward gain of *H*(s)

Now let us apply Barkhausen criterion to the *LC* VCOs. Figure 15 shows simplified schematics of basic cross coupled *LC* VCOs at the oscillation frequency. Since inductor and capacitor are not seen (equivalent impedance becomes infinite) at the oscillator frequency, excluded.

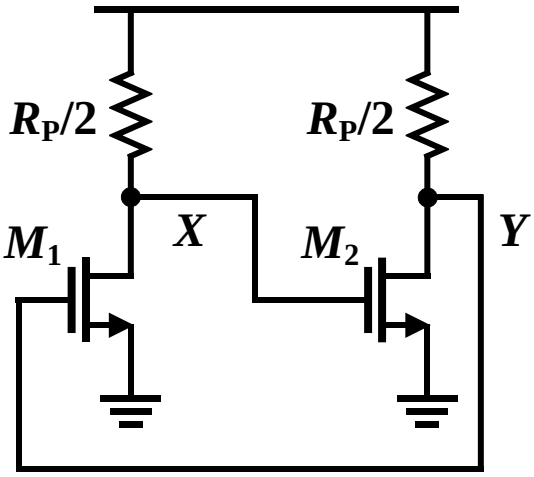

Figure 15. Simplified schematics of *LC* VCOs at resonance frequency

Only parallel resistor is seen at the drain node. Now, it becomes two stage common source amplifiers. Each stage contributes -π with gain of $-g_m \cdot R_P/2$. From node X to node Y, this circuit shifts phase -2π. To meet the Barkhausen criterion, open loop gain has to greater or equals to 1.

$$\left(\frac{g_m \cdot R_P}{2}\right)^2 \geq 1 \tag{15}$$

This equation can be rewritten.

$$R_P \geq \frac{2}{g_m} \tag{16}$$

This inequality implies that to securely ensure the start up of *LC* VCOs, Q-factor of tank and transconductance of g_m cell should be large.

The other approach is negative resistance. This approach also can have the same result as the Barkhausen criterion.

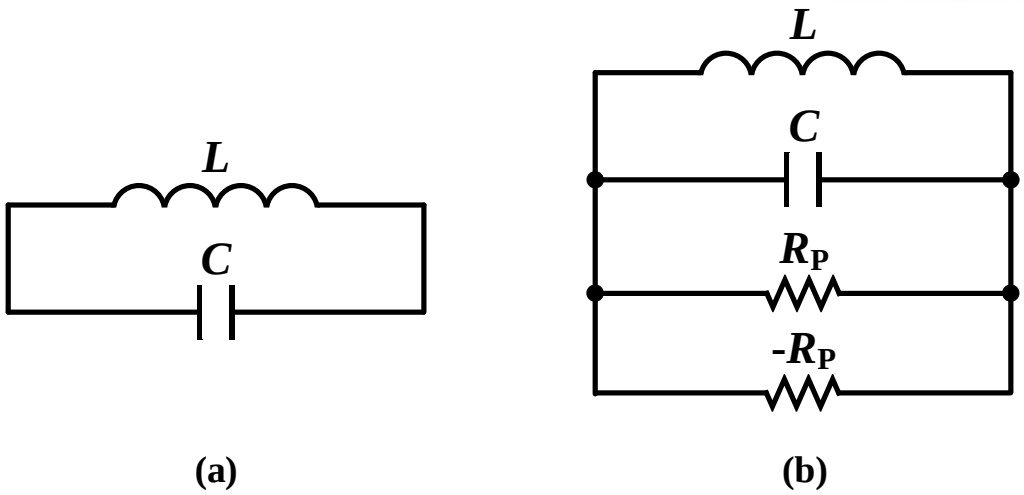

Figure 16. (a) Ideal *LC* tank and (b) Lossy *LC* tank with negative resistance

Likewise figure 16(a), ideal *LC* tank must oscillate without any addon circuits. However, in practical lossy tank, parasitic resistance dissipates power. Therefore, compensation is necessary for the continuous oscillation. As shown in figure 16(b), R_p and $-R_p$ are canceled each other so that only ideal inductor and capacitor are remain that can sustain oscillation similar to (a).

Then how is possible to have negative resistance? the answer is using cross coupled topology.

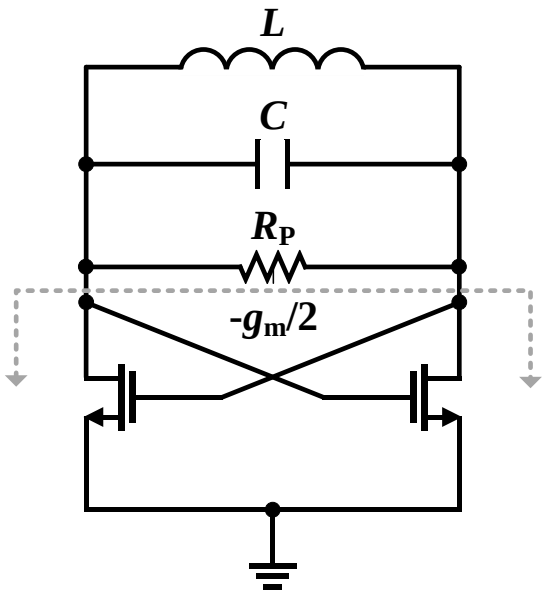

Figure 17. *LC* VCO topology by one-port view

As shown in figure 17, the impedance seen to the cross coupled transistors is negative. For the oscillation occur, negative resistance must cancel R_P as inequalities below.

$$R_P \| \left(-\frac{g_m}{2}\right) \leq 0$$

$$R_P \geq \frac{2}{g_m} \tag{17}$$

This result is exactly same as the that of Barkhausen criterion. In both cases suggest for the stable oscillation, g_m and R_p should be sufficiently large.

4.4. *LC* VCO TOPOLIGIES

The efforts to improve phase noise and power efficiency brought new structures such as [8]-[9]. However, only consider class-B topology which is most widely used in commercial products. We are going to compare NMOS and CMOS type cross coupled class-B *LC* VCOs.

NMOS-type class-B *LC* VCOs

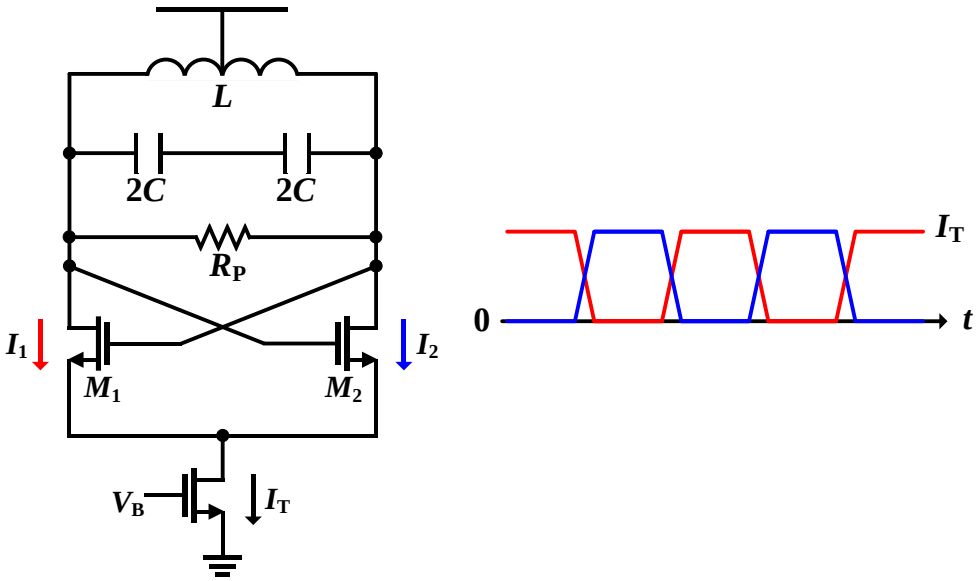

Figure 18. Simplified architecture of NMOS-type *LC* VCOs and its current waveform in steady state

Figure 18 shows the structure of NMOS-type *LC* VCOs and its current waveform. VCOs consists of an *LC* tank, a cross coupled pair, and a tail current source. As shown in the current waveform, current steered on one side and on the other side and its conduction angle is π. It is possible to decompose current waveform into common mode and differential mode waveform. As shown in figure 19, summation of common mode and differential mode current becomes total current waveform.

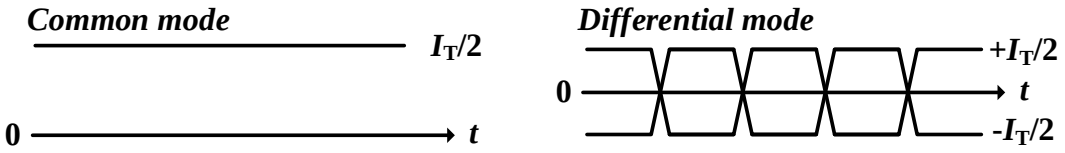

Figure 19. Common mode and Differential mode current waveform of NMOS-type *LC* VCO

The differential mode current waveform can be expressed by using Fourier series. Since the tank's inherent filter characteristic, harmonics are rejected and only fundamental tone is injected to the tank. The voltage swing is made by the current and parallel resistance. Thus, the voltage swing of single branch can be expressed as below.

$$V_{\mathrm{OUT}} = \frac{R_P}{2} \cdot \frac{2}{\pi} \cdot I_{\mathrm{T}} \cdot \sin 2\pi f \tag{18}$$

Here, the swing of VCOs is determined by I_T since R_P is mainly determined by the tank. No matter how we increase the amount of tail current, voltage swing cannot exceed the supply voltage. This is called voltage limited region. In voltage limited region, as current increases, voltage swing does not change and only additional power is wasted, results in degradation of FOM. On the other hand, when voltage swing increases as current increases, it is called current limited region. In current limited region, as current increases, phase noise performance improves at the expense of power consumption. It is important to choose optimal operation region to elicit maximum performance from the devices.

CMOS-type class-B *LC* VCOs

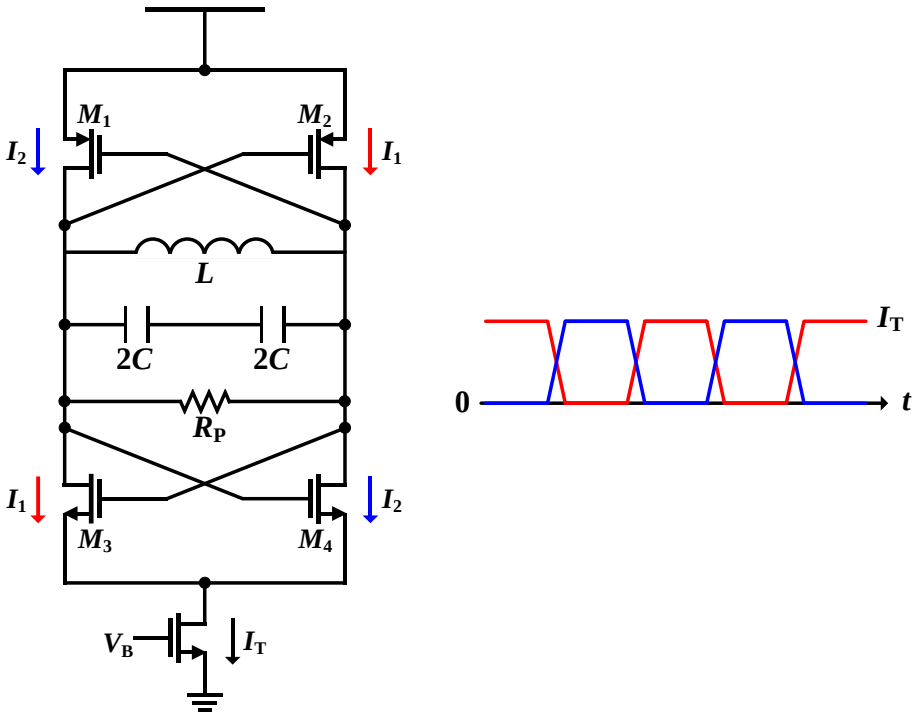

Figure 20. Simplified architecture of CMOS-type LC VCOs and its current waveform in steady state

Figure 20 shows the structure of CMOS-type *LC* VCOs and its current waveform. VCOs consists of an *LC* tank, two cross coupled pair, and a tail current source. As shown in the current waveform, current steered left PMOS and right NMOS, right PMOS and left NMOS transistors turn on and off staggered and its conduction angle is π. It is possible to decompose current waveform into common mode and differential mode waveform as NMOS-type did. As shown in figure 21, common mode current does not exist and differential mode current only exists.

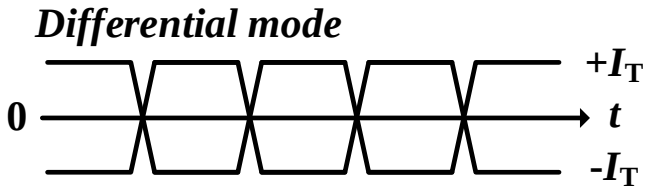

Figure 21. Differential mode current waveform of CMOS-type *LC* VCO

In the same way as NMOS-type, the differential mode current waveform can be expressed by using Fourier series. The voltage swing is made by the current and parallel resistance. Thus, the voltage swing of single branch can be expressed as below.

$$V_{OUT} = \frac{R_P}{2} \cdot \frac{4}{\pi} \cdot I_T \cdot \sin 2\pi f \tag{19}$$

Mostly same as NMOS-type, but current. CMOS-type has twice current since common mode current does not exist. The concept of voltage limited region and current limited region is exactly same.

Comparison between NMOS-type and CMOS-type *LC* VCO

Based on previous analysis on the types of *LC* VCO, let us compare the characteristics.

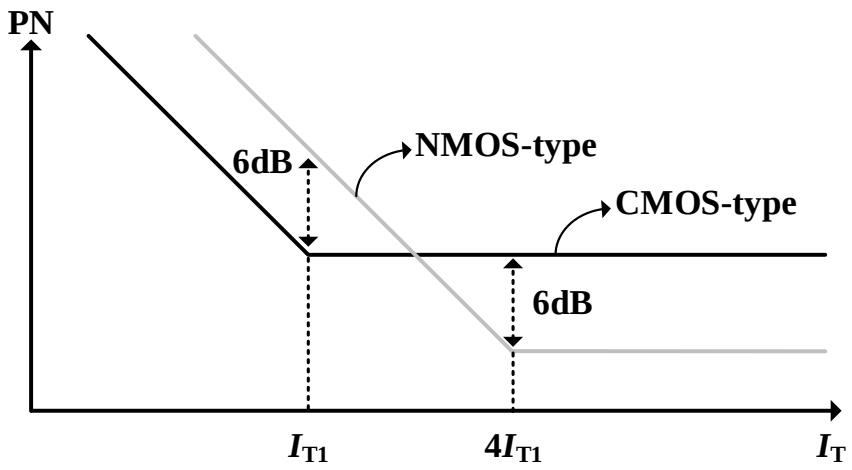

Figure 22. Comparison of phase noise (PN) performance between NMOS-type and CMOS-type *LC* VCO

As shown in figure 22, phase noise of CMOS-type saturates earlier than that of NMOS-type. That is because, NMOS-type has twice maximum voltage swing and has half current. At the optimal points, NMOS-type has lower achievable phase noise since its voltage swing is twice of supply voltage. However, both types of VCOs have same maximum FOM since power consumption of NMOS is larger. Up to applications, choose optimal topology is important. NMOS-type has better phase noise performance and lower parasitic capacitance but lower power efficiency. While, CMOS-type has better power efficiency and twice transconductance but more parasitics.

4.5. PHASE NOISE IN *LC* VCOS

This subchapter, two aspects of phase noise model will be introduced. One is Lesson's equation and the other is impulse-sensitive function.

4.5.1. LEESON'S PHASE NOISE MODEL

The Leeson's phase noise model equation is the most famous analysis of phase noise [10]. Leeson assumes two things in the equation. That is, the VCOs is LTI system and noise is only come from the *LC* tank. In reality, neither the VCO is LTI system or only the tank has noise. However, by these assumptions, it is sufficient to the equation follows the overall tendency and understand phase noise.

Here, derivation of Leeson's equation. At first, small deviation from the resonance frequency, the impedance of the *LC* tank is:

$$Z(\omega_O + \Delta\omega) \approx j \cdot \frac{\omega_O L}{2\frac{\Delta\omega}{\omega_O}} \tag{20}$$

ω_o is the oscillation frequency of the tank. Substituting that $Q = R_P/(\omega_o L)$

$$|Z(\omega_O + \Delta\omega)| \approx R_P \cdot \frac{\omega_O}{2Q\Delta\omega} \tag{21}$$

And the noise is

$$\frac{\overline{v_n^2}}{\Delta f} = \frac{\overline{i_n^2}}{\Delta f} \cdot |Z|^2 = 4kTR_P \left(\frac{\omega_O}{2Q\Delta\omega}\right)^2 \tag{22}$$

Divide by the signal power and take a logarithm, then phase noise is given by

$$\mathcal{L}(\Delta\omega) = 10\log\left[\frac{2kT}{P_{signal}} \cdot \left(\frac{\omega_O}{2Q\Delta\omega}\right)^2\right] \tag{23}$$

Later, Leeson modified phase noise model to include a flicker noise dominant region and flat region

(24)

$$\mathcal{L}(\Delta\omega) = 10\log\left[\frac{2FkT}{P_{\text{signal}}}\cdot\left(1+\left(\frac{\omega_{\text{O}}}{2Q\Delta\omega}\right)^2\right)\cdot\left(1+\left(\frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\right)\right)\right]$$

Where the factor F is a fitting parameter rather than physical concepts. $\Delta\omega_{1/f3}$ denotes a flicker noise corner frequency. This equation assumed $1/f^3$ corner and $1/f^2$ corner are exactly occurred at $1/f$ corner however in real cases, it is not. Although, this equation is very simple and intuitive, it is difficult to know the effect of other parameters which is not included in this equation. This equation is further become a foundation of FOM of oscillator.

4.5.2. IMPULSE-SENSITIVE FUNCTION (ISF) MODEL

The previous analysis was based on LTI approximation. However, oscillators are very nonlinear in steady state and its operation is time varying. Therefore, more accurate analysis is needed. Hajimiri et al. proposed the concept of impulse-sensitive function (ISF) that is LTV model [11]. They assumed noise to phase transfer function is linear and noise is time varying.

When the current impulse is injected to the tank, the tank experiences amplitude and phase distortion. The impulse has a very high frequency components then all the capacitors are considered as short and all the inductors are considered as open.

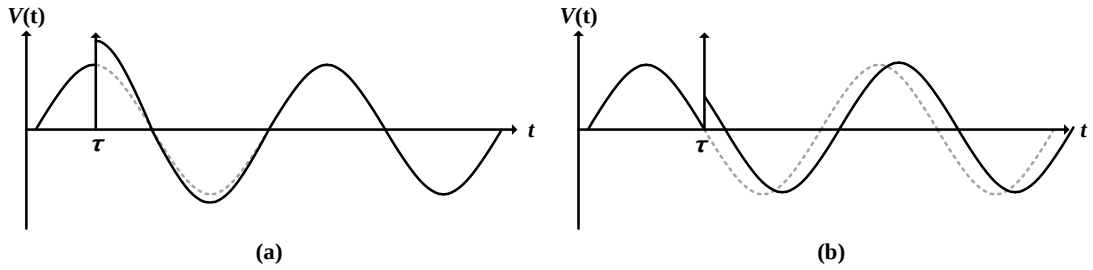

Figure 23. Impulse response of the *LC* VCOs (a) when impulse is at the peak (b) when impulse is at the zero crossing

Figure 23 shows the current impulse injecting to the tank then amplitude and phase shift. When impulse is injected to the tank at the peak, only amplitude changes and it recovers over several terms. While, when the impulse is injected to the tank at the zero crossing, phase is shifted. In this case, shifted phase cannot be recovered. In one period, there is sensitive points and robust points as impulse injected. And phase distortion function is linear function of current injection. Then the impulse response for the phase distortion is:

$$h_{\Phi}(t,\tau) = \frac{\Gamma(\omega_{O}\tau)}{q_{\max}} u(t - \tau) \tag{25}$$

Where q_{max} is the peak charge and u(t-τ) is the unit step function. The gamma function, Γ(ω_{O}τ) is the Impulse sensitivity function (ISF). It is to say, the magnitude of ISF is proportional to the sensitivity. Which means, the VCOs are vulnerable to noise when the magnitude of ISF is large. ISF can be usually expressed the form of derivative of its signal.

5. DESIGN OF 12−14.5 GHZ DIGITALLY-CONTROLLED OSCILLATOR (DCO) FOR ULTRA-LOW-JITTER PLL

5.1. OBJECTIVE AND MOTIVATIONS

For the ultra-low-jitter digital PLL, the quantization noise minimization is critical issue. Therefore, designing a high-resolution DCO is very important. To raise the resolution of DCOs, several methods are proposed such as [1]-[3]. For the design simplicity and robustness, delta sigma DAC based DCO is designed.

5.2. DESIGN OF DELTA-SIGMA DAC

To sufficiently suppress the quantization noise, high-resolution delta sigma DAC is required. The resolution of DSM can be increased at the expense of power consumption, the resolution of DAC can be increased at the expense of linearity. The resolution is differently set to the proportional path and integral path of the digital PLL. In both paths, the resolution of the DSM is 12-bit. Proportional path has 5-bit RDAC and integral path has 6-bit RDAC. Since noise shaping of the 2rd order DSMs, 2rd order low pass filter is necessary. Pole frequency of proportional path is 500kHz and that of integral path is 100MHz. At the optimal pole frequencies, the quantization noise is negligible at the PLL output and filter area is minimal. The pole frequencies are also related to the operation frequency of DSM, that is 400MHz.

For the noise shaping, 12-bit multi stage noise shaping (MASH) 1-1 DSM is used. Figure 24 shows the block model of MASH 1-1 DSM. By the cascading, second order noise shaping is realized.

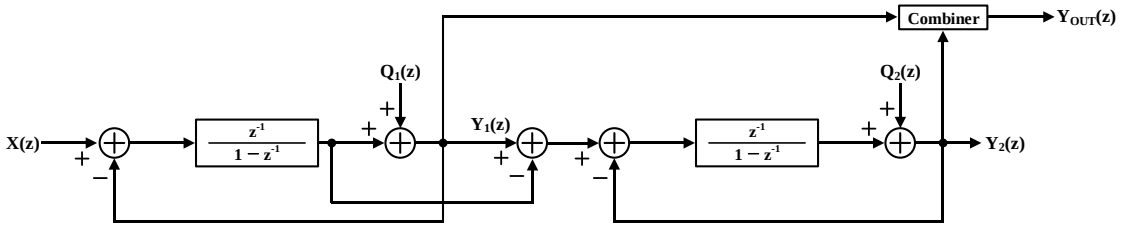

Figure 24. Linear block model of MASH 1-1 DSM

RDACs used simple string topology for simple design. Linearity of RDAC is not a critical issue in this application. So, linearity is specification is somewhat relieved. Since the order of DSM is two, we need 4 input (+1, 0, -1, -2) at each bit to make a fractional value. Therefore, for n-bit RDAC, total 2^n + 4 resistors are needed for a second order DSM.

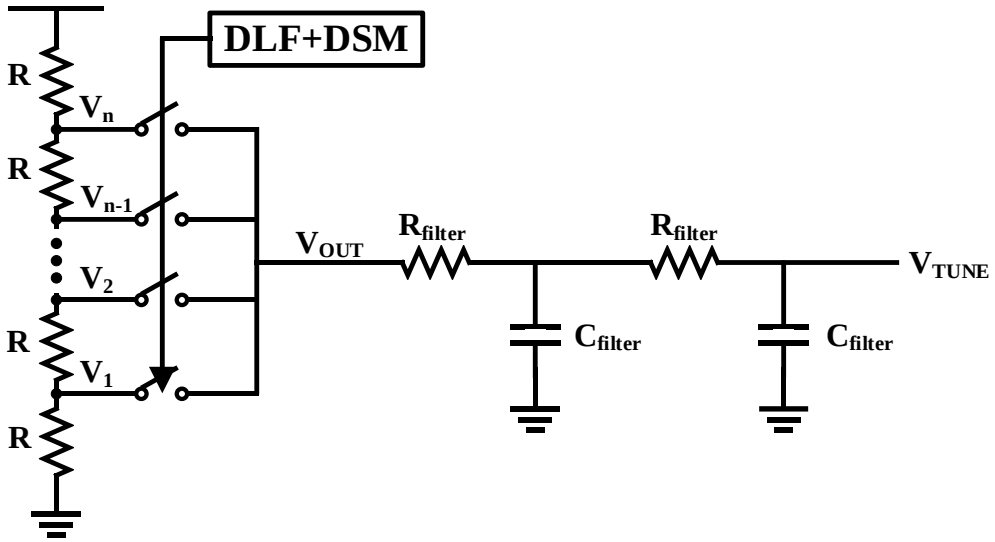

Figure 25. Schematics of delta-sigma RDAC with 2nd order low pass filter and DLF used in integral path

Figure 25 shows the schematics of delta-sigma DAC and output low pass filter with digital loop filter (DLF). The resistance of unit resistor of the DAC is 180Ohm. The nominal high voltage of DAC is 1.2V. So that the static power of the DAC is under 100μW.

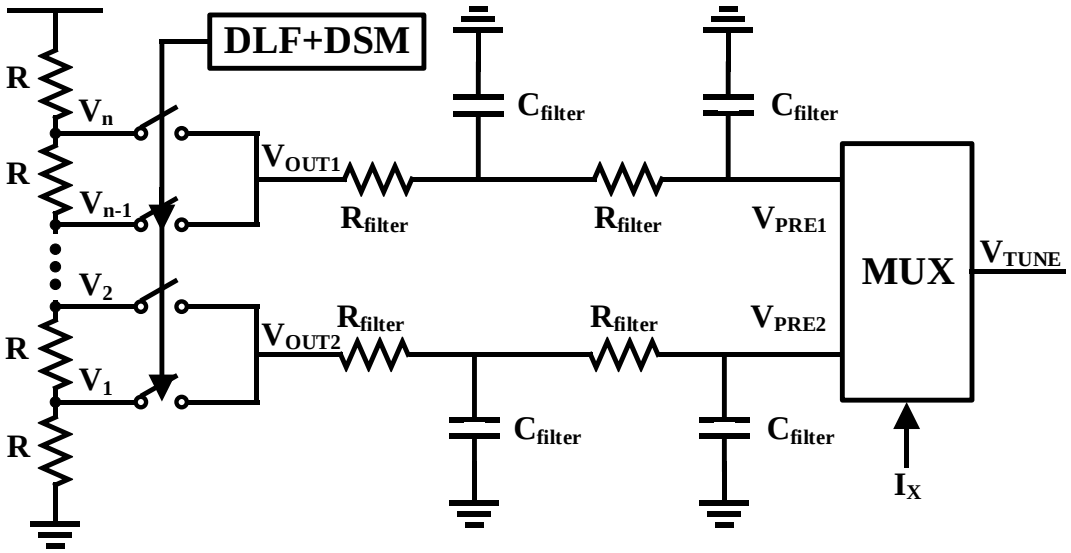

Figure 26. Schematics of delta-sigma RDAC with 2nd order low pass filters, output MUX and DLF used in proportional path

Figure 26 shows the schematics for delta-sigma DAC and low pass filters, MUX with digital loop filter (DLF). Unlike the design of integral path, in proportional path, DAC is divided into half, upper and lower part. Upper part and lower part receive input separately and the inputs are complementary. Therefore, two 2^{nd} order low pass filters are needed. I_X denotes the decision signal from the bang-bang phase detector. It determines which voltage will be used for the control voltage, V_{TUNE}. The dimension of resistors in the DAC is 145Ohm. Likewise, nominal voltage high of the DAC is 1.2V. Therefore, the static power is 280μW.

5.3. DESIGN OF *LC* VCO

Designing high performance *LC* VCOs are crucial since the performance of the oscillator determines overall performance of the PLL. The given requirements are to achieve ultra-low jitter digital PLL.

Frequency tuning range: 12-14.5GHz
KVCO: 50MHz/V for main loop, 500MHz/V for axillary loop
Power: < 5mW
FOM: -184dB @ 1MHz frequency offset

Since the target frequency is high, g_m cell of the VCO should be thin transistor to reduce parasitic capacitance. Also, CMOS-type topology is chosen because, in the NMOS-type *LC* VCO with thin transistor, gate oxide easily breaks. For the superior phase noise performance, hvt device is used for the g_m cell to prevent the transistors are operate in deep triode region.

The first step of design is determination of dimension of inductor. The value of inductance is related to the oscillation frequency, frequency tuning range, phase noise performance, and power consumption. Therefore, selecting optimal inductance is a milestone of the VCO. In this design, 200pH of inductor is used and its shape is calculated to have maximum Q-factor. The calculated Q-factor is 30 at 14GHz.

Next step is designing a capacitor bank (CBANK) for coarse frequency tuning. The total number of bits are 7 then, frequency resolution of coarse tuning becomes 20MHz/bit; this induce about 2.5fF of unit capacitance. The 7-bit CBANK is binary weighted.

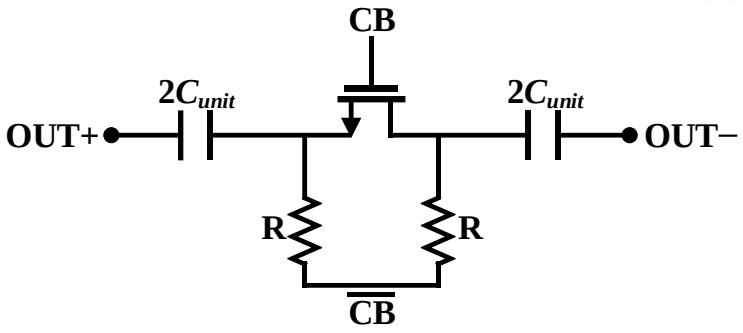

Figure 27. Schematics of CBANK unit

Figure 27 shows the schematics of unit capacitor bank. Where OUT+, OUT- are VCO outputs, C_{unit} is unit capacitor, bias resistor, R and enable signal CB. When CB is 1, unit capacitors are seen to the tank. Whereas, when CB is 0, only parasitic capacitance of transistor is seen to the tank. For a distinguishable switching, R should be sufficiently large and R_{on} of transistor should be small. Usually the pole frequency of inherent high pass filter is 20 times larger than the oscillation frequency. As the W/L ratio of the transistor increases, Q-factor of CBANK increases as the R_{on} decreases. However, parasitic capacitance increases as well which decreases maximum oscillation frequency. Therefore, finding the optimal point is important. The value of R is 100kOhm and size of transistor is 800n/60n. Since the CBANK is binary weighted, R becomes half and transistor size becomes twice as the bit increase.

Once the CBANK design is done, determine dimension of the varactor to meet given KVCO specification. Figure 28 shows the schematics of varactors in *LC* VCO. It consists of DC block capacitors, varactors, and bias resistors. Varactors are thick device since the leakage current of thin device is significant which causes reference spurs in PLL. DC block capacitors are 0.5pF, resistors are 4.5kOhm.

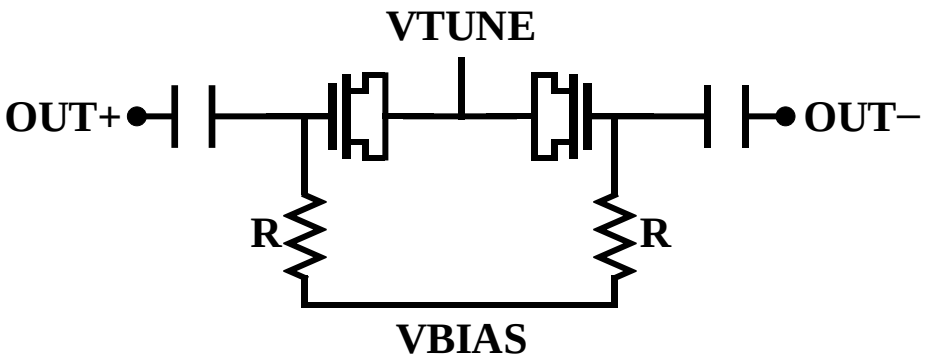

Figure 28. Schematics of varactors in *LC* VCO

For the main loop, to make 50MHz/V of KVCO, capacitance of the varactor is 22-28fF. In the same way, for the auxiliary loop, to make 50MHz/V of KVCO, capacitance of the varactor is 124-192fF.

The size of gm cell is directly related to the overall frequency, start-up, noise and power of the VCO. The most important one is start-up. Usually, we usually set start-up margin about 3 times larger than the Barkhausen criterion to ensure the oscillation of VCO under PVT variations. After satisfy start-up margin by changing W/L ration, next step is changing the dimension of the cell. Larger W·L value leads lower flicker noise corner but it also decreases the frequency. By the several simulations, transistor dimension is fixed to 27u/100n.

Design of *LC* VCO is endless loop. To meet the given specifications, unabated iteration is required. Even if the layout is done, we have to go back to the schematics level unless the specifications are satisfied.

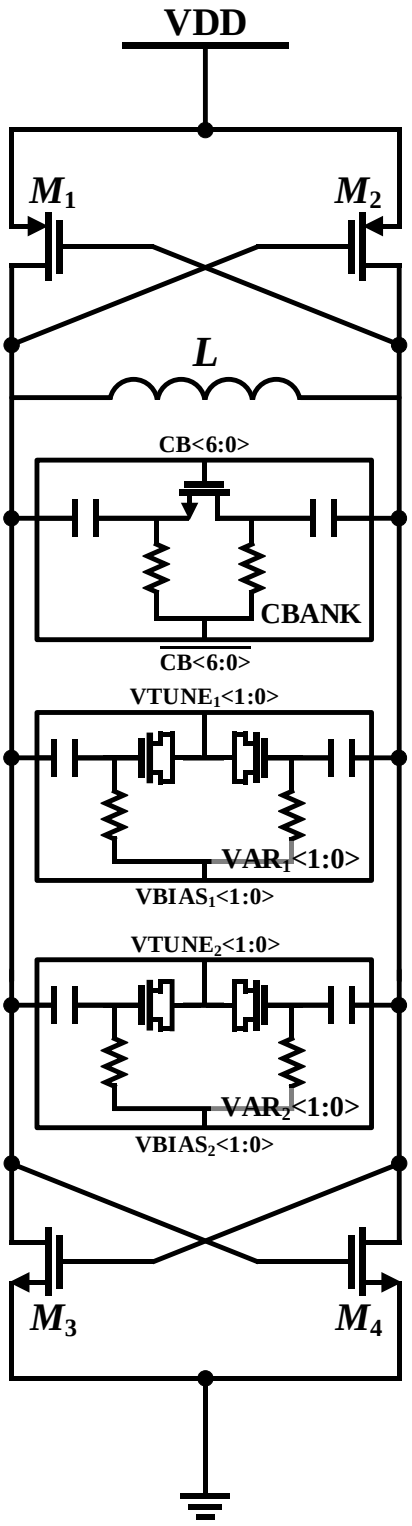

Figure 29. Schematics of the CMOS-type *LC* VCO with frequency tuner

Figure 29 shows the final version of the *LC* VCO. In consists of a CMOS type g_m cell, a spiral inductor, a 7-bit CBANK, two varactors (VAR_1) for main loop with 50MHz/V KVCO, two varactors (VAR_2) for auxiliary loop with 500MHz/V KVCO.

5.4. SIMULATION AND EXPERIMENTAL RESULTS

Delta-sigma DAC

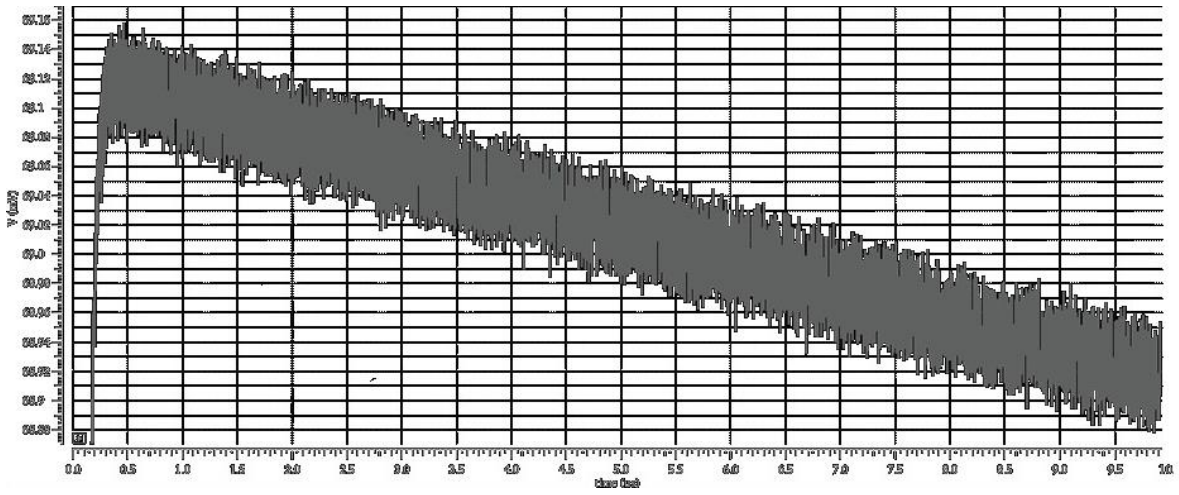

Figure 30. Transient response of the out of DSM DAC and low pass filter

Figure 30 shows the output transient result of DSM DAC after low pass filter. As the input code of the DAC decreases, output of the low pass filter decreases as well. Thanks to the DSM, resolution of the DAC is significantly increased and the low pass filter filtered out the high frequency components. The remained ripples are negligible at the output of the PLL.

***LC* VCO**

Figure 31 shows the simulation results of the worst-case R_P. The solid line is schematic simulation result and the dash line is PEX simulation result. Because of the parasitic capacitance, in PEX simulation, the R_P is reduced from 115Ohm to 97Ohm compared to that of schematic simulation. g_m of the CMOS cross coupled transistor is 30.5mS. Therefore, in schematic, start-up margin is about 3 and in PEX, start-up margin is nearly less than 3. In both cases, oscillation is guaranteed with sufficient start-up margin.

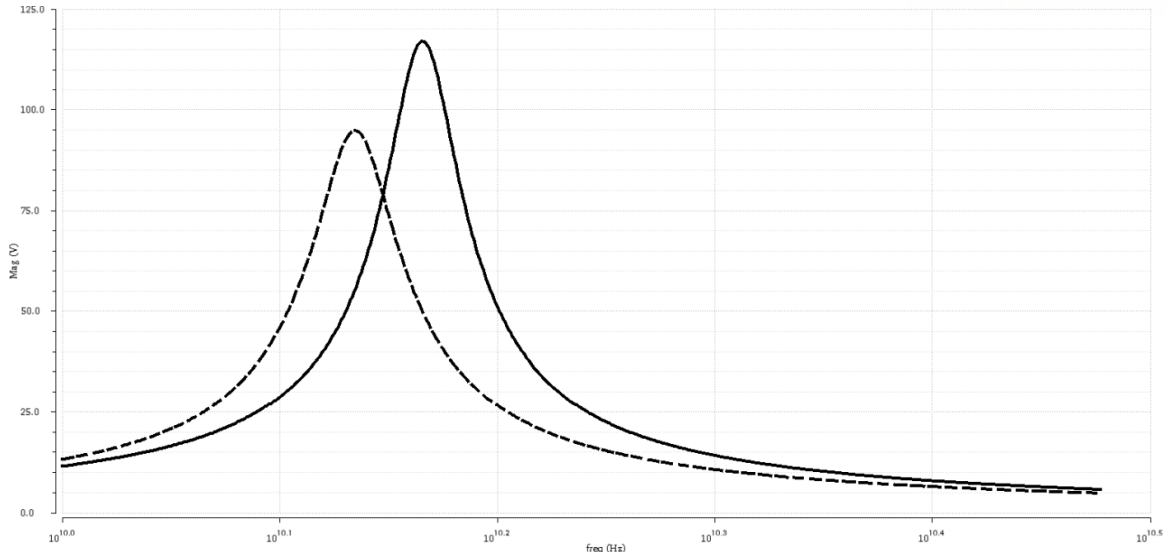

Figure 31. Simulation results of the worst-case RP

Figure 32 show simulation results of frequency tuning range. Likewise, solid line is schematic and dash line is PEX results. In schematic, frequency tuning range is 14-18.5GHz which is higher than the target frequency to prepare frequency decreasing induced by parasitic capacitance in layout. However, frequency tuning range is still high in PEX simulation result, 13.5-15.8GHz. That is because, the PEX results cannot count parasitic inductance but capacitance. Also, dummy metal can decrease oscillation frequency.

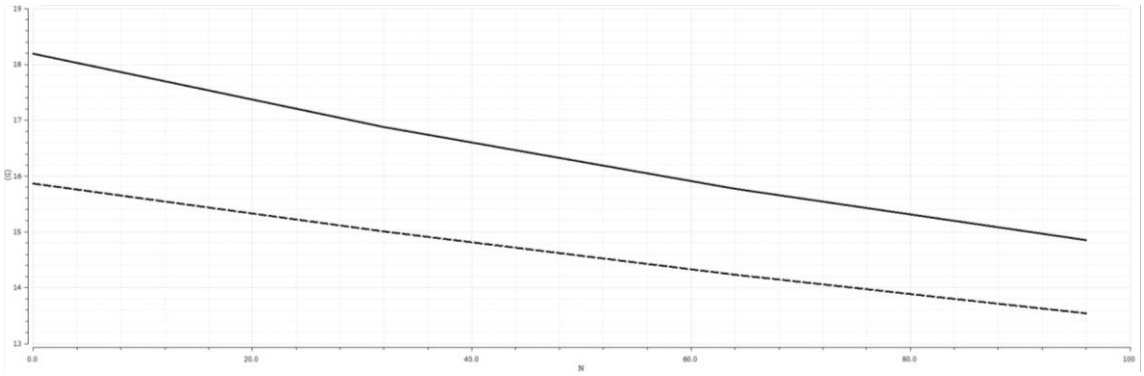

Figure 32. Simulation results of frequency tuning range

Figure 33 shows KVCO simulation results at 14GHz. As shown in the graph, both KVCO of main loop and auxiliary loop meet the target specification, 52MHz/V and 550MHz/V for each. Although is it slightly higher than the target, we can manage it with VBIAS.

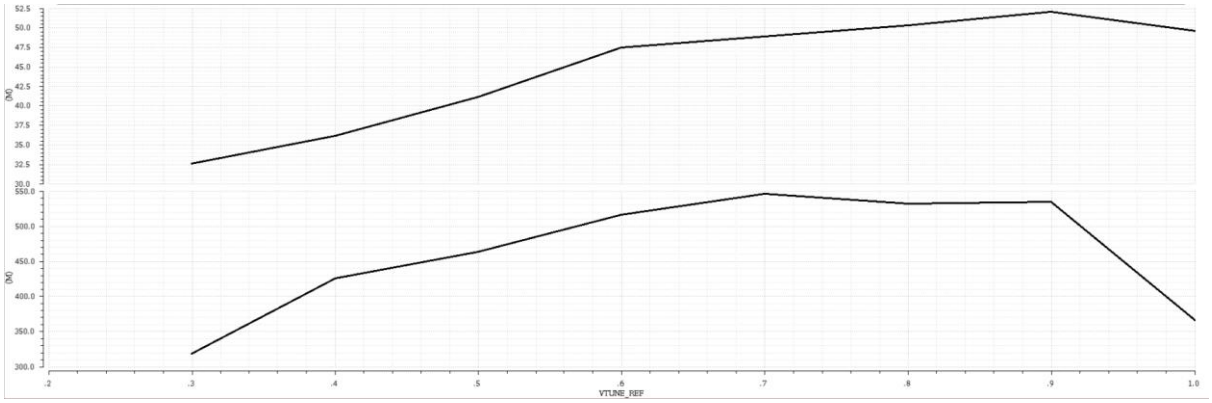

Figure 33. Simulation results of KVCO of (up) main loop (down) auxiliary loop when VTUNE is changed from 0.2 to 1.0V

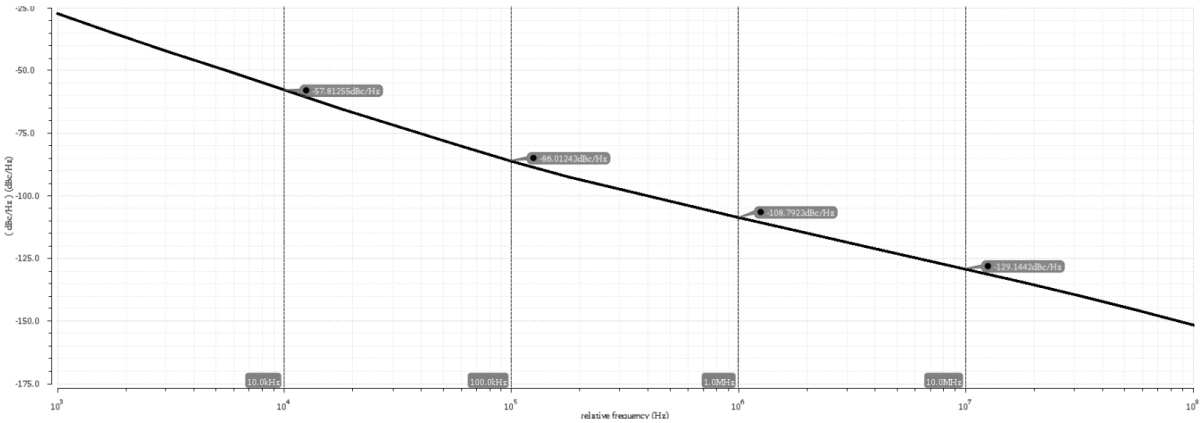

Figure 34. Simulation results of the output phase noise @ 14.2GHz in schematic

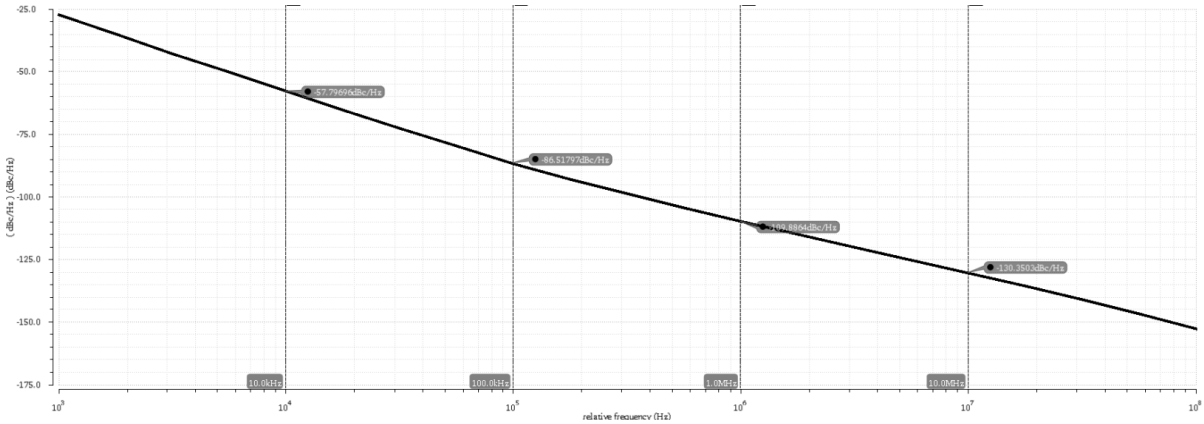

Figure 34. Simulation results of the output phase noise @ 13.2GHz in PEX

Figure 33 and 34 show the phase noise results of schematic and PEX simulation. In both cases, CBANK code is fixed to 127 which is all the capacitor units are on. The flicker noise corner is less than 500kHz which does not degrade the jitter performance of the PLL. At 1MHz frequency offset, phase noise is -108.8dBc/Hz and -109.9dBc/Hz for schematic and PEX each. The power consumption was 5.3mW for both cases. The FOM of the VCO at 1MHz frequency offset is -184.8dB and -184.9dB for each schematic and PEX. So that target FOM is satisfied in both cases.

In the measurements, the frequency was nearly 10% decreased from the PEX results. This is the effect of parasitic inductance and dummy metal that PEX does not count. This amount of degradation is expected resulted. The maximum frequency fells to 14.5

GHz from 15.8GHz and the minimum frequency fells to 12GHz from 13.5GHz. Figure 35 shows the measured phase noise graph at 14GHz.

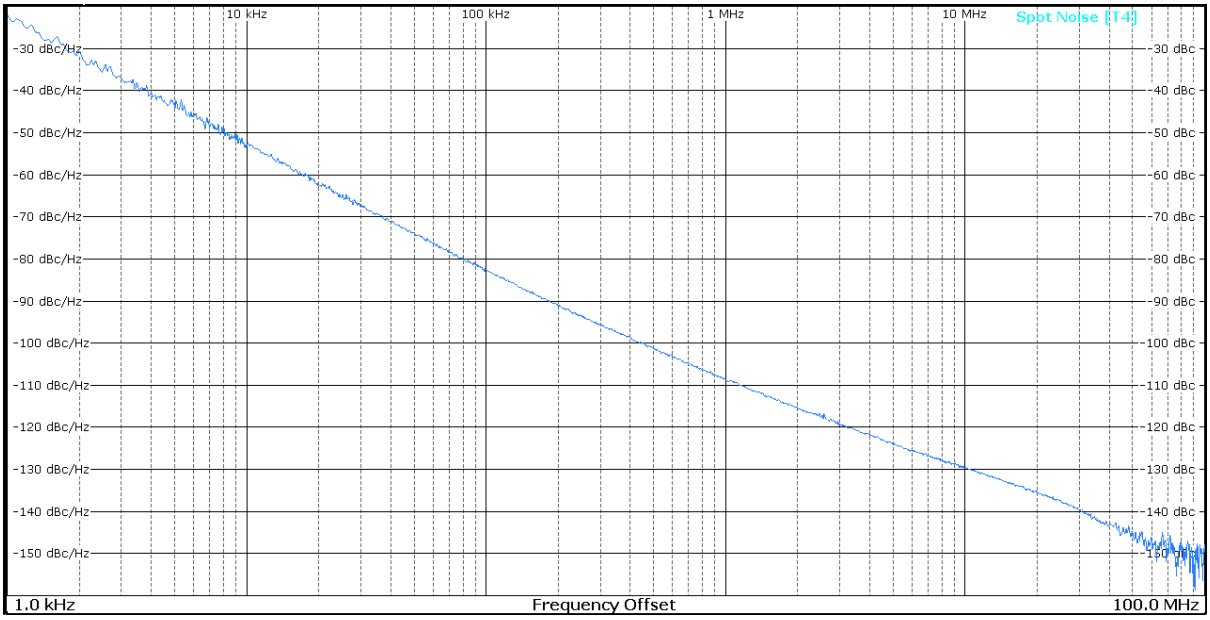

Figure 35. Measured phase noise graph at 14GHz

The FOM of the VCO at 1MHz frequency offset is less than 184dB when phase noise is -109dBc/Hz and power consumption was 5.5mW. This measured result meets the design target specifications.

6. CONCLUSIONS

In this thesis, the fundamentals of the DCO including DAC, DSM, VCO were introduced and the design of low phase noise, high resolution DCO were discussed.

The DCO was designed for the ultra-low-jitter digital sub sampling PLL. To suppress the enormous amount of quantization noise, very fine frequency resolution is critical. Also, phase noise of the *LC* VCO itself is crucial for ultra-low-jitter applications. For the high-performance *LC* VCO design, understanding of the basic insight of the oscillator is needed. The DCO consists of string type RDAC, MASH 1-1 DSM, and CMOS-type cross coupled *LC* VCO. The frequency resolution is significantly increased by using DSM. The proportional path has the resolution of 17-bit, while the integral path has the resolution of 18-bit. The DSM is operating at 400MHz and its quantization noise is canceled by the 2^{nd} order low pass filter at the output of the DAC. By adopting 2^{nd} order noise shaping, quantization noise at PLL out is negligible. The DAC designed with a string resistor topology for its design simplicity and relieved target specifications. The DCO has 12-14.5GHz of frequency tuning range. The phase noise at 1MHz offset frequency is -109dBC/Hz at 14GHz output. The average power consumption is 5.5mW. Calculated FOM at 1MHz offset frequency is -184.5dB.

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